



MOTOROLA

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

The MC14511B BCD-to-seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test (\overline{LT}), blanking (\overline{BI}), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Low Logic Circuit Power Dissipation
- High-Current Sourcing Outputs (Up to 25 mA)
- Latch Storage of Code
- Blanking Input
- Lamp Test Provision
- Readout Blanking on all Illegal Input Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Facility
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Chip Complexity: 216 FETs or 54 Equivalent Gates

MAXIMUM RATINGS (Voltages referenced to V_{SS}).

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	V
Input Voltage, All Inputs	V_{in}	-0.5 to $V_{DD} + 0.5$	V
DC Current Drain per Input Pin	I	10	mA
Operating Temperature Range - AL Device CL/CP Device	T_A	-55 to +125 -40 to -85	°C
Storage Temperature Range	T_{stg}	-65 to -150	°C
Maximum Output Drive Current (Source) per Output	I_{OHmax}	25	mA
Maximum Continuous Output Power (Source) per Output †	P_{OHmax}	50	mW

† $P_{OHmax} = I_{OH} (V_{DD} - V_{OH})$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. A destructive high current mode may occur if V_{in} and V_{out} are not constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (See Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MC14511B

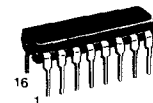
CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER



L SUFFIX
CERAMIC PACKAGE
CASE 620



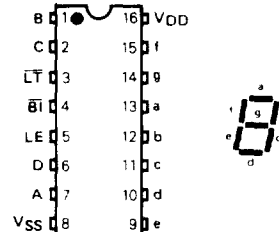
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: -55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

PIN ASSIGNMENT



TRUTH TABLE

INPUTS						OUTPUTS								
LE	\overline{BI}	\overline{LT}	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
X	X	0	X	X	X	X	1	1	1	1	1	1	1	B
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	0	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	0	1	0	2
0	1	1	0	1	0	0	1	1	1	1	0	0	0	3
0	1	1	1	0	0	0	1	1	0	0	1	1	0	4
0	1	1	1	0	0	1	1	0	1	1	0	1	1	5
0	1	1	1	0	1	0	0	0	1	1	1	0	0	6
0	1	1	1	1	0	0	1	1	1	0	0	0	0	7
0	1	1	1	1	0	1	1	1	1	1	1	1	1	8
0	1	1	1	1	1	0	0	0	0	0	0	0	0	9
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	1	1	1	1	X	X	X	X	X	X	X	Blank

X = Don't Care
* Depends upon the BCD code previously applied when LE = 0

MC14511B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}^*		25°C			T_{high}^*		Unit			
			Min	Max	Min	Typ	Max	Min	Max				
Output Voltage $V_{in} = V_{DD}$ or 0	"0" Level V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	V			
		10	—	0.05	—	0	0.05	—	0.05				
		15	—	0.05	—	0	0.05	—	0.05				
	"1" Level $V_{in} = 0$ or V_{DD}	V_{OH}	5.0	4.1	—	4.1	4.57	—	4.1	—	V		
			10	9.1	—	9.1	9.58	—	9.1	—			
			15	14.1	—	14.1	14.59	—	14.1	—			
Input Voltage [#]	"0" Level V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	V			
		10	—	3.0	—	4.50	3.0	—	3.0				
		15	—	4.0	—	6.75	4.0	—	4.0				
	"1" Level V_{IH}	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	V		
			10	7.0	—	7.0	5.00	—	7.0	—			
			15	11.0	—	11.0	8.25	—	11.0	—			
Output Drive Voltage (AL Device) Source	V_{OH}	5.0	4.10	—	4.10	4.57	—	4.1	—	V			
			$I_{OH} = 0$ mA	—	—	—	4.24	—	—		—		
			$I_{OH} = 5.0$ mA	—	—	—	4.12	—	3.5		—		
			$I_{OH} = 10$ mA	3.90	—	3.90	3.94	—	—		—		
			$I_{OH} = 15$ mA	—	—	—	3.70	—	3.0		—		
			$I_{OH} = 20$ mA	3.40	—	3.40	3.54	—	—		—		
		10	$I_{OH} = 0$ mA	9.10	—	9.10	9.53	—	9.1	—	V		
			$I_{OH} = 5.0$ mA	—	—	—	9.25	—	—	—			
			$I_{OH} = 10$ mA	9.00	—	9.00	9.17	—	8.6	—			
			$I_{OH} = 15$ mA	—	—	—	9.04	—	—	—			
			$I_{OH} = 20$ mA	8.60	—	8.60	8.90	—	8.2	—			
			$I_{OH} = 25$ mA	—	—	—	8.70	—	—	—			
		15	$I_{OH} = 0$ mA	14.1	—	14.1	14.59	—	14.1	—	V		
			$I_{OH} = 5.0$ mA	—	—	—	14.27	—	—	—			
			$I_{OH} = 10$ mA	14.0	—	14.0	14.13	—	13.6	—			
			$I_{OH} = 15$ mA	—	—	—	14.07	—	—	—			
			$I_{OH} = 20$ mA	13.6	—	13.6	13.95	—	13.2	—			
			$I_{OH} = 25$ mA	—	—	—	13.70	—	—	—			
		Output Drive Voltage (CL/CP Device) Source	V_{OH}	5.0	4.10	—	4.10	4.57	—	4.1	—	V	
					$I_{OH} = 0$ mA	—	—	—	4.24	—	—		—
					$I_{OH} = 5.0$ mA	—	—	—	4.12	—	3.3		—
					$I_{OH} = 10$ mA	3.60	—	3.60	3.94	—	—		—
					$I_{OH} = 15$ mA	—	—	—	3.75	—	2.5		—
					$I_{OH} = 20$ mA	2.80	—	2.80	3.54	—	—		—
10	$I_{OH} = 0$ mA			9.10	—	9.10	9.58	—	9.1	—	V		
	$I_{OH} = 5.0$ mA			—	—	—	9.26	—	—	—			
	$I_{OH} = 10$ mA			8.75	—	8.75	9.17	—	8.45	—			
	$I_{OH} = 15$ mA			—	—	—	9.04	—	—	—			
	$I_{OH} = 20$ mA			8.10	—	8.10	8.90	—	7.8	—			
	$I_{OH} = 25$ mA			—	—	—	8.75	—	—	—			
15	$I_{OH} = 0$ mA			14.1	—	14.1	14.59	—	14.1	—	V		
	$I_{OH} = 5.0$ mA			—	—	—	14.27	—	—	—			
	$I_{OH} = 10$ mA			13.75	—	13.75	14.18	—	13.45	—			
	$I_{OH} = 15$ mA			—	—	—	14.07	—	—	—			
	$I_{OH} = 20$ mA			13.1	—	13.1	13.95	—	12.8	—			
	$I_{OH} = 25$ mA			—	—	—	13.80	—	—	—			
Output Drive Current (AL Device) Sink	I_{OL}			5.0	0.64	—	0.51	0.88	—	0.36	—	mA	
				$V_{OL} = 0.4$ V	10	1.6	—	1.3	2.25	—	0.9		
				$V_{OL} = 0.5$ V	15	4.2	—	3.4	8.8	—	2.4		
				$V_{OL} = 1.5$ V	—	—	—	—	—	—	—		
Output Drive Current (CL/CP Device) Sink	I_{OL}			5.0	0.52	—	0.44	0.88	—	0.36	—	mA	
				$V_{OL} = 0.4$ V	10	1.3	—	1.1	2.25	—	0.9		
		$V_{OL} = 0.5$ V	15	3.6	—	3.0	8.8	—	2.4				
		$V_{OL} = 1.5$ V	—	—	—	—	—	—	—				

(Continued)

MC14511B

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	V _{DD} Vdc	T _{low} *		25°C			T _{high} *		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Input Current (AL Device)	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA
Input Current (CL/CP Device)	I _{in}	15	—	±0.3	—	±0.00001	±0.3	—	±1.0	μA
Input Capacitance	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (AL Device) (Per Package) V _{in} =0 or V _{DD} , I _{out} = 0 μA	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μA
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Quiescent Current (CL/CP Device) (Per Package) V _{in} =0 or V _{DD} , I _{out} = 0 μA	I _{DD}	5.0	—	20	—	0.005	20	—	150	μA
		10	—	40	—	0.010	40	—	300	
		15	—	80	—	0.015	80	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.9 μA/kHz) f + I _{DD}						μA	
		10	I _T = (3.8 μA/kHz) f + I _{DD}							
		15	I _T = (5.7 μA/kHz) f + I _{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.

T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level =

1.0 Vdc min @ V_{DD} = 5.0 Vdc

2.0 Vdc min @ V_{DD} = 10 Vdc

2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF.

I_T(C_L) = I_T(50 pF) + 3.5 × 10⁻³ (C_L - 50) V_{DD}f

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc,
and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V _{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time t _{TLH} = (0.40 ns/pF) C _L + 20 ns t _{TLH} = (0.25 ns/pF) C _L + 17.5 ns t _{TLH} = (0.20 ns/pF) C _L + 15 ns	t _{TLH}	5.0	—	40	80	ns
		10	—	30	60	
		15	—	25	50	
Output Fall Time t _{THL} = (1.5 ns/pF) C _L + 50 ns t _{THL} = (0.75 ns/pF) C _L + 37.5 ns t _{THL} = (0.55 ns/pF) C _L + 37.5 ns	t _{THL}	5.0	—	125	250	ns
		10	—	75	150	
		15	—	65	130	
Data Propagation Delay Time t _{PLH} = (0.40 ns/pF) C _L + 620 ns t _{PLH} = (0.25 ns/pF) C _L + 237.5 ns t _{PLH} = (0.20 ns/pF) C _L + 165 ns t _{PHL} = (1.3 ns/pF) C _L + 655 ns t _{PHL} = (0.60 ns/pF) C _L + 260 ns t _{PHL} = (0.35 ns/pF) C _L + 182.5 ns	t _{PLH}	5.0	—	640	1280	ns
		10	—	250	500	
		15	—	175	350	
	t _{PHL}	5.0	—	720	1440	
		10	—	290	580	
		15	—	200	400	
Blank Propagation Delay Time t _{PLH} = (0.30 ns/pF) C _L + 585 ns t _{PLH} = (0.25 ns/pF) C _L + 187.5 ns t _{PLH} = (0.15 ns/pF) C _L + 142.5 ns t _{PHL} = (0.85 ns/pF) C _L + 442.5 ns t _{PHL} = (0.45 ns/pF) C _L + 177.5 ns t _{PHL} = (0.35 ns/pF) C _L + 142.5 ns	t _{PLH}	5.0	—	600	750	ns
		10	—	200	300	
		15	—	150	220	
	t _{PHL}	5.0	—	485	970	
		10	—	200	400	
		15	—	160	320	
Lamp Test Propagation Delay Time t _{PLH} = (0.45 ns/pF) C _L + 290.5 ns t _{PLH} = (0.25 ns/pF) C _L + 112.5 ns t _{PLH} = (0.20 ns/pF) C _L + 80 ns t _{PHL} = (1.3 ns/pF) C _L + 248 ns t _{PHL} = (0.45 ns/pF) C _L + 102.5 ns t _{PHL} = (0.35 ns/pF) C _L + 72.5 ns	t _{PLH}	5.0	—	313	625	ns
		10	—	125	250	
		15	—	90	180	
	t _{PHL}	5.0	—	313	625	
		10	—	125	250	
		15	—	90	180	
Setup Time	t _{su}	5.0	100	—	—	ns
		10	40	—	—	
		15	30	—	—	
Hold Time	t _h	5.0	60	—	—	ns
		10	40	—	—	
		15	30	—	—	
Latch Enable Pulse Width	t _{WL}	5.0	520	260	—	ns
		10	220	110	—	
		15	130	65	—	

*The formulas given are for the typical characteristics only.

MC14511B

FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORMS

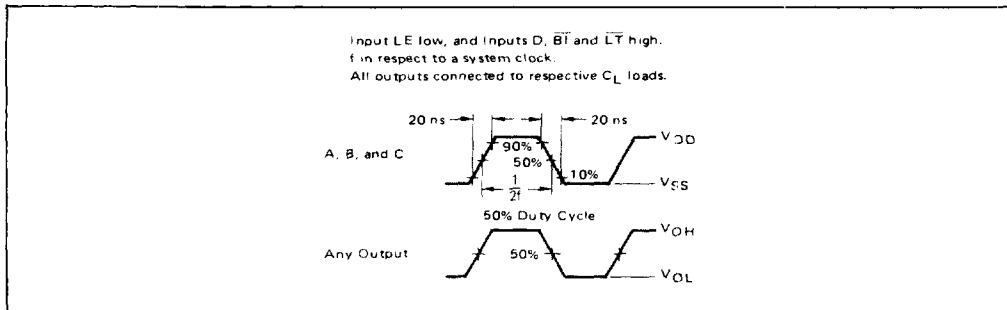
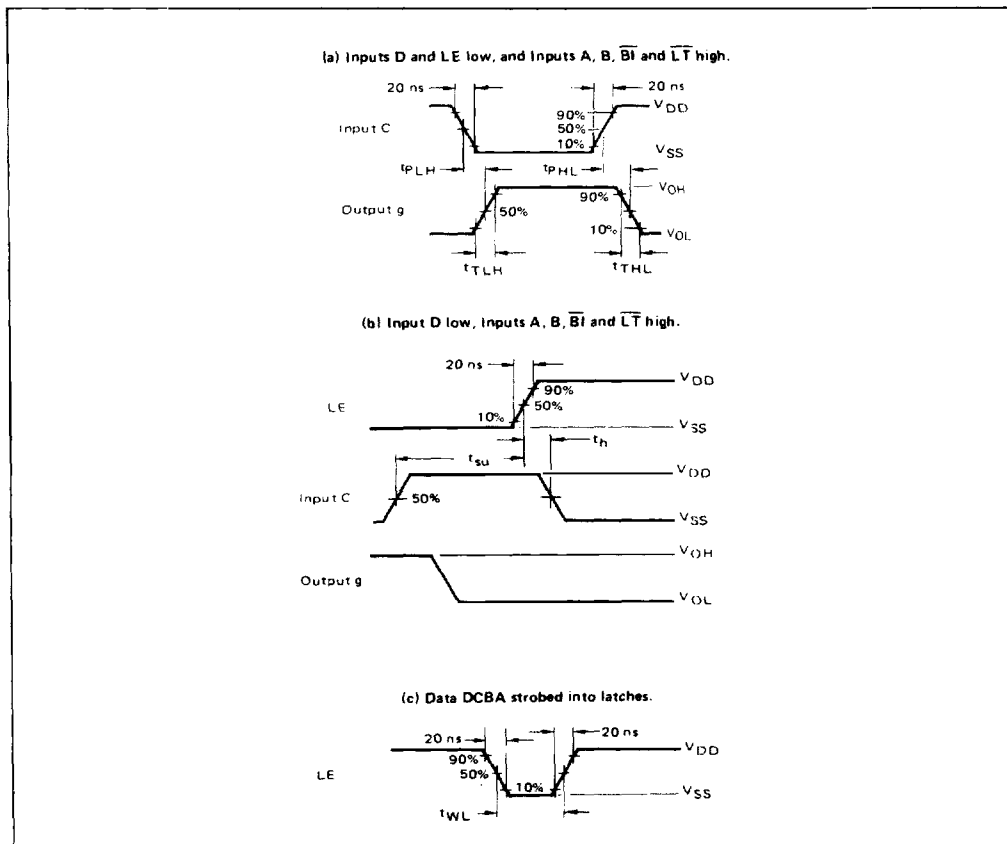
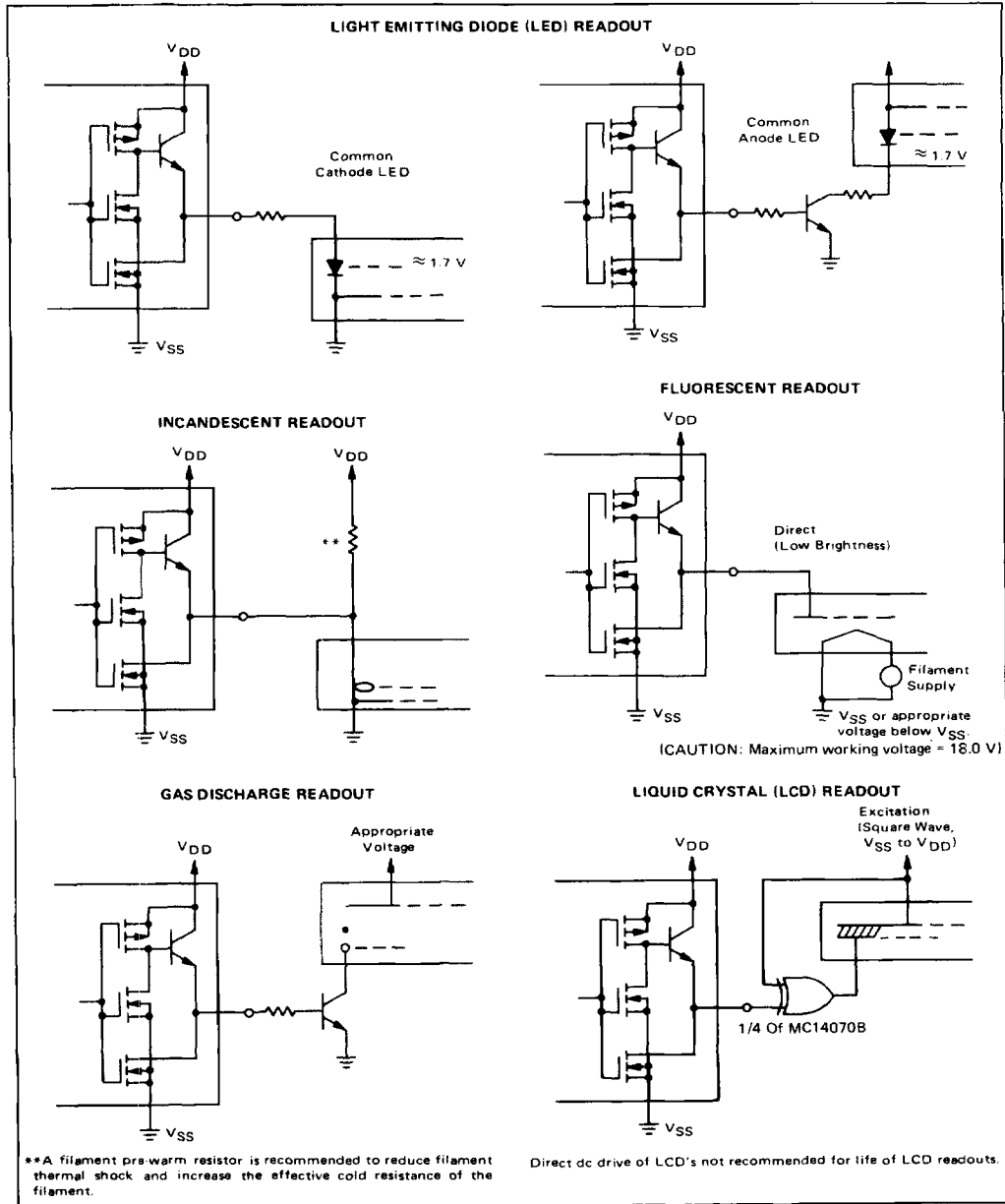


FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS



MC14511B

CONNECTIONS TO VARIOUS DISPLAY READOUTS



6

MC14511B

LOGIC DIAGRAM

